REMARKS

Please reconsider the application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering the application.

Disposition of Claims

Claims 4, 16, and 27 are pending in the present application, and claims 4, 16, and 27 are independent. By way of this reply, claims 4, 16, and 27 have been amended to clarify the claim language. Support for these amendments can be found, for example, in paragraphs [0151] and [0154] of the published specification. Further, claims 16 and 27 have been amended to more clearly recite hardware elements. Support for these amendments can be found, for example, in paragraphs [0203], [0206], [0224], and [0238] of the published specification and in Figures 20, 21, 29 and 35. Claims 4, 16, and 27 have been further amended to correct minor informalities. No new matter has been added by way of these amendments.

Objection(s) to the Claims

Claims 4, 16, and 27 were objected to for informalities. By this reply, correction has been made as suggested by the Examiner. Accordingly, withdrawal of this objection is respectfully requested.

Rejection(s) Under 35 U.S.C § 101

Claims 16 and 27 stand rejected under 35 U.S.C. §101 as being directed to non-statutory subject matter. By way of this reply, claims 16 and 27 have been amended to more clearly recite hardware elements such as a power supply and memory unit. Accordingly, the

amended claims are directed to statutory subject matter. In view of the above, withdrawal of this rejection is respectfully requested.

Rejection(s) Under 35 U.S.C § 103

Claims 4, 16, and 27 stand rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,043,672 ("Sugasawara"). As noted above, claims 4, 16, and 27 have been amended. To the extent that the rejection still applies to the amended claims, this rejection is respectfully traversed.

One or more embodiments disclosed in this application are directed to a method and apparatus for detecting defects of an integrated circuit by using a transient power supply current of the circuit under test. As explained in paragraph [0087] of the published specification with reference to Figure 1, the transient power supply current is the current that flows in the device when the test pattern changes. By measuring transient power supply currents of a circuit, the user can determine whether and where the circuit has defects. More specifically, in accordance with one embodiment explained in paragraphs [0170]-[0173] with reference to Figures 14 and 15, a fault location list for a test pattern sequence is generated, and the fault locations in the list are assumed to be defective when the transient power supply currents are detected abnormal. Applicant already explained in detail at pp. 5-6 of the Request for Continued Examination filed May 30, 2008 as to how such fault location lists are used in determining the locations of defects.

Advantageously, such fault location lists can be employed in testing circuits to easily find where defective elements are located. Further, unlike prior art, the claimed invention can presume fault locations without electrically isolating sections in the device under test.

Accordingly, independent claims 4 and 16 require, in part, "measuring...a *transient power supply current* generated on said semiconductor IC in accordance with the change of said test pattern and determining whether said *transient current* shows abnormality or not" (emphasis added). In addition, independent claim 27, as amended, recites "measuring...a *transient power supply current* generated on said semiconductor IC in accordance with the change of said test pattern" and "determining that said *transient current* is abnormal in a case that the time integral of said transient power supply current is over a predetermined value" (emphasis added).

Sugasawara is directed to a test apparatus that introduces dedicated power lines to each region of interest on an IC in order to isolate defects. Sugasawara, unlike the claimed invention, discloses test equipment that measures the *quiescent current* that flows when a device under test is in a static DC condition. At page 4 of the instant Office Action, the Examiner appears to regard the quiescent current of Sugasawara as the same as the transient current of the claimed invention. However, this is incorrect because quiescent current and transient current are two very different concepts. Specifically, in column 2, lines 12-18, Sugasawara discloses the following:

> When testing quiescent current with a functional test set, the tester is generally halted at predetermined test steps suitable for quiescent current testing. Once halted (i.e., no transistor state switching is occurring) the power supply of the device under test is measured by the ATE and the resulting value is compared to predetermined reference values or test limits.

In column 6, lines 28-29, Sugasawara further discloses that "[i]n the static test state, the circuits within an integrated circuit 10 consume quiescent currents." From these descriptions, it is clear that quiescent current, as the term is used in Sugasawara, does not refer to

the transient current of the claimed invention, which flows when the test pattern changes. In addition, unlike the claimed invention, Sugasawara requires electrical isolation of sections in the device under test in order to determine which sections are defective.

Therefore, Sugasawara fails to show or suggest at least "measuring...a *transient power supply current* generated on said semiconductor IC in accordance with the change of said test pattern and determining whether said *transient current* shows abnormality or not," as required by claims 4 and 16, and at least "measuring...a *transient power supply current* generated on said semiconductor IC in accordance with the change of said test pattern" and "determining that said *transient current* is abnormal in a case that the time integral of said transient power supply current is over a predetermined value," as required by claim 27.

Furthermore, Sugasawara also fails to teach or suggest the "transient power supply current is determined to be abnormal in a case that *the time integral of said transient power supply current is over a predetermined value*," as required by claim 4, "determines that said transient power supply current is abnormal in a case that *the time integral of said transient power supply current* is over a predetermined value," as required by claim 16, and "determining that said transient current is abnormal in a case that *the time integral of said transient power supply current* is over a predetermined value," as required by claim 27.

At page 4 of the instant Office Action, the Examiner alleges that this feature is taught by Sugasawara in column 2, lines 38-41. However, the cited passage in Sugasawara merely discloses that "[i]n order to isolate the defective area of an integrated circuit, a failure analysis engineer seeks to determine which section of the integrated circuit is responsible for unusual current levels." In fact, Sugasawara is completely silent with regard to using a time integral of said transient power supply current.

In view of the above, Sugasawara fails to show all limitations of independent claims 4, 16, and 27. Thus, Claims 4, 16, and 27 are patentable over Sugasawara. Accordingly, withdrawal of this rejection is respectfully requested.

Conclusion

Applicant believes this reply is fully responsive to all outstanding issues and places this application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 02008/071003).

Dated: October 31, 2008

Respectfully submitted,

By_____

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Attachments